AF/RW

[2207/12121]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Examiner: Akash Saxena
Eric M. MONROE	
For: TECHNIQUE FOR DEFINING PROBABILISTIC RELIABILITY TEST REQUIREMENTS	
Filed: October 17, 2001	
	Art Unit 2128
Serial No.: 09/982,061	

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Date: 10/27/06 . Reg. No. 53,443
Signature: Michael P. Paul

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APPEAL BRIEF TRANSMITTAL IN RESPONSE TO A NOTICE OF NON-COMPLIANCE

SIR:

Accompanying this Appeal Brief Transmittal is a Replacement Appeal Brief pursuant to 37 C.F.R. § 41.37 **(in triplicate as a courtesy)** for filing in the above-identified patent application, in response to the Notification of Non-Compliance mailed on September 28, 2006.

*It is noted that the appropriate appeal brief of fee of **$500.00**, which is the Appeal Brief fee under 37 C.F.R. § 1.17(c) was already paid when the first Appeal Brief was mailed on September 19, 2006 (and filed on September 21, 2006) and therefore should not be charged again to the extent already charged.*

The Commissioner is also authorized, as necessary and/or appropriate, to charge any additional and appropriate fees, including any further Rule 136(a) extension fees, or credit any overpayment to Deposit Account No. **11-0600**. Two duplicate copies of this transmittal are enclosed for these purposes.

Respectfully submitted,

Dated: 10/27/06

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[02207/12121]

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Date: 10/27/06

Signature: Michael P. Ball

REPLACEMENT APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

S I R:

In the above-identified patent application ("the present application"), the Appellant mailed a Notice of Appeal on March 14, 2006 from the Final Office Action issued by the United States Patent and Trademark Office on October 14, 2005. This Notice of Appeal was received by the Patent Office on March 17, 2006.

In the Final Office Action, claims 1 to 22 were finally rejected. An Advisory Action was mailed on January 10, 2006.

The Appeal Brief filed on September 21, 2006 (and mailed on September 19, 2006) in support of the appeal of the final rejections of the claims was deemed non-compliant in the Notification of Non-Compliant Appeal Brief of September 28, 2006.

It is respectfully submitted that all matters have been corrected and that this Replacement Appeal Brief complies with 37 CFR 41.37.

For the reasons more fully set forth below, the final rejection of claims 1 to 22 should be reversed.

1. REAL PARTY IN INTEREST

The real party in interest in the present appeal is Intel Corporation, 2200 Mission College Boulevard, P.O. Box 58119, Santa Clara, California, 95052-8119. Intel Corporation is the assignee of the entire right, title, and interest in the above-identified application.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences "which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal."

3. STATUS OF CLAIMS

Claims 1 to 5 and 16 stand finally rejected under 35 U.S.C. § 103(a) as being obvious over "Intel Technology Journal Q3" by Nicholas P. Mencinger et al. ("Mencinger") in view of "Application Specific Semiconductor Device Qualification Methodology" by M. Doty ("Doty").

Claims 6 to 12, 14 and 17 to 22 stand finally rejected under 35 U.S.C. § 103(a) as being obvious over Mencinger in view of Doty and "ReliaSoft's ALTA 1.0 On Site Training Guide" ("ReliaSoft").

Claims 13 and 15 stand finally rejected under 35 U.S.C. § 103(a) as being obvious over Mencinger in view of Doty, ReliaSoft and "Semiconductor Device Reliability Failure Models by Ted Dellin et al. ("Dellin").

Appellant appeals from the final rejection of claims 1 to 22. A copy of the appealed claims is attached hereto in the Appendix..

4. STATUS OF AMENDMENTS

In response to the Final Office Action issued on October 14, 2005, an Amendment was filed on December 14, 2005. The Amendment did not include any amendments to the claims.

It is understood for purposes of this appeal that any Amendments to date have already been entered by the Examiner.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 relates to a computer-implemented method, tangibly embodied on a computer readable storage medium, which when executed will quantify the

reliability test requirements of a package/chip device over a product lifetime. The computer-implemented method includes modeling a plurality of different types of ambient and power-driven temperature cycle fluctuations the package/device is expected to undergo over the product lifetime (See page 8, line 1 to page 10, line 12, and Figure 3, which schematically illustrates the temperature and power use of an exemplary package/chip used in a particular market segment over time in respective graphs 90 and 100), and determining the accelerated life test requirements that represent each of the plurality of different types of temperature cycles fluctuations (See page 10, line 14 to page 12, line 4, and Figure 4, which shows a modified Coffin-Manson empirical model that calculates the number of accelerated test cycles 205 required to account for temperature fluctuations in each of the temperature fluctuation regimes 206, 207 and 208).

Similarly, independent claims 4 and 19 are directed, respectively, to a method of relating accelerated life test parameters used to assess reliability of a package/chip device to expected frequencies and magnitudes of temperature cycle fluctuations encountered by the package/chip device over a product lifetime, and to an article comprising a computer-readable storage medium which stores instructions. Here, the method and instructions include defining a particular market application use for the package/chip device (See, Market Segment box 80 of Figure 2, and page 7, lines 8 to 11, which state that using the Market Segment box 80, the user can choose between CPU and non-CPU market types, such as Desktop, Laptop, Workstation, Telecommunications, Handheld devices, Personal Digital Assistants (PDA), Cellular, etc.), quantifying expected frequencies and magnitudes of temperature fluctuations of the package/chip device in each of a plurality of temperature cycle fluctuation regimes, based in part on the particular market application use of the package/chip device (See page 7, lines 12 to 16, which state that the market segment determines the product environment of the package/chip and the consumer use patterns associated with the product – for example, since laptops typically contain a smaller fan they are subject to higher temperatures than desktops, and since servers are generally kept on constantly except during maintenance they do not undergo as many on/off cycles as other types), and incorporating the quantified expected frequencies and magnitudes of the temperature fluctuations of the package/chip device in each of the temperature regimes into an accelerated life model (See Figures 3, 4 and page 10, lines 14 to 15, which state that when the magnitude and frequency of the temperature fluctuation events have been fully accounted for and estimated, these values are input into an accelerated life model such as the Coffin-Manson empirical model of Figure 4).

Claim 16 relates to a method of systematically quantifying representative field use conditions associated with a particular product having a package/chip device. Here, the method includes defining a product market segment (See, Market Segment box 80 of Figure 2 and page 7, lines 8 to 11), defining a shipping route taken by the product and identifying temperature cycle fluctuations and power cycles fluctuations encountered by the package /chip of the product (See, Shipping Path entry box 82 of Figure 2 and page 7, lines 19 to 21, which state that the user selects the shipping route that determines the environment that the package/chip will experience en route from the chip manufacturer to a product assembly site to a reseller), and quantifying frequencies and magnitudes of temperature fluctuations pertinent to each identified ambient and power driven temperature fluctuation, wherein the frequencies and magnitudes are based in part on the product market segment and the shipping route (See Figures 3, 4, and page 10, lines 14 to 23, which state that according to the Modified Coffin-Manson model, the total number accelerated reliability cycles required to accurately model the temperature profile of the package/chip device is equivalent to a sum of, *inter alia*, the number of cycles to separately model temperature fluctuations due to shipping cycles, both ground and air, and the number of cycles require to separately model power cycle fluctuations including on/idle, application use, and market segment; See also, page 11, lines 15 to 20, which refer to a corresponding temperature fluctuation ratio to be applied to each of six usage cycle terms: storage 210, shipping air 211, shipping ground 212, application use 213, on/idle 214 and operating transport 215).

6. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1 to 5 and 16 are obvious over Mencinger in view of Doty.

B. Whether claims 6 to 12, 14 and 17 to 22 are obvious over Mencinger in view of Doty and ReliaSoft.

C. Whether claim 13 and 15 are obvious over Mencinger in view of Doty, ReliaSoft and Dellin.

7. ARGUMENTS

A. Claims 1 to 5 and 16 are not obvious over Mencinger in view of Doty.

Claims 1 to 5

Claims 1 to 5 and 16 stand finally rejected under 35 U.S.C. § 103(a) as being obvious over Mencinger in view of Doty. It is respectfully submitted that none of claims 1 to 5 is obvious over these references for at least the following reasons.

Claim 1 relates to a computer-implemented method to quantify the reliability test requirements of a package/chip device over a product lifetime, the method including modeling a plurality of different types of ambient and power-driven temperature cycle fluctuations the package/device is expected to undergo over the product lifetime, and determining the accelerated life test requirements that represent each of the plurality of different types of temperature cycles fluctuations.

Claim 4 relates to a method of relating accelerated life test parameters used to assess reliability of a package/chip device to expected frequencies and magnitudes of temperature cycle fluctuations encountered by the package/chip device over a product lifetime, the method including defining a particular market application use for the package/chip device, quantifying expected frequencies and magnitudes of temperature fluctuations of the package/chip device in each of a plurality of temperature cycle fluctuation regimes, based in part on the particular market application use of the package/chip device, and incorporating the quantified expected frequencies and magnitudes of the temperature fluctuations of the package/chip device in each of the temperature regimes into an accelerated life model.

In contrast to claims 1 and 4, Mencinger refers to a mechanism-based methodology for processor package assessments, in which failure mechanisms are modeled with the appropriate physical model. In this regard, Mencinger does not disclose, or even suggest, determining accelerated life test requirements that represent ***each*** of a plurality of different types of temperature cycles fluctuations a package/device is expected to undergo ***over the product lifetime***, as recited by claim 1, or incorporating into the accelerated life model quantified expected frequencies and magnitudes of temperature fluctuations of a package/chip device in ***each*** of a plurality of temperature regimes ***over the product lifetime***, as recited by claim 4. Indeed, the Office Action admits on pages 6 and 8 that Mercinger does not teach a plurality of temperature cycle fluctuation regimes nor accelerated life test requirements for all situations. Accordingly, Mencinger fails to disclose, or even suggest, the features of claims 1 and 4 with respect to determining the accelerated life test requirements that represent each of the plurality of different types of temperature cycles fluctuations a package/device is expected to undergo over a product lifetime, or incorporating into an

accelerated life model quantified expected frequencies and magnitudes of temperature fluctuations of the package/chip device in each of a plurality of temperature regimes over the product lifetime.

Also in contrast to claims 1 and 4, Doty refers to a strategy for implementation of application specific characterization/qualification involving four application phases. See Slides 1 to 3. In this regard, Doty does not disclose, or even suggest, determining accelerated life test requirements that represent ***each*** of a plurality of different types of temperature cycle fluctuations a package/device is expected to undergo ***over a product lifetime***, or incorporating into an accelerated life model quantified expected frequencies and magnitudes of temperature fluctuations of a package/chip device in ***each*** of a plurality of temperature regimes ***over the product lifetime***. Instead, Doty simply refers to an application-specific semiconductor qualification methodology, in which certain stress conditions are provided that refer to temperature cycle fluctuations for only one application phase, namely, the ***operation life*** phase, but not in ***each*** of the four application phases. See Slide 3, which refers to a temperature range and a number of cycles for the "Package Temp Cycle", "Interconnect Temp Cycle" and "Power Cycle" only for the ***operation*** life phase of the package/chip. In this regard, it is respectfully submitted that Doty does not consider temperature or power cycle fluctuations of other non-operational phases referred to on Slide 3, in particular, "Assembly" and "Storage/Transportation", which would presumably also occur over a product lifetime.

Accordingly, Doty also fails to disclose, or even suggest, the features of claims 1 and 4 with respect to determining the accelerated life test requirements that represent each of the plurality of different types of temperature cycles fluctuations a package/device is expected to undergo over a product lifetime, or incorporating into an accelerated life model quantified expected frequencies and magnitudes of temperature fluctuations of the package/chip device in each of a plurality of temperature regimes over the product lifetime.

In rejecting a claim under 35 U.S.C. § 103(a), the Office Action bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of

success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

As explained above, the combination of Mencinger and Doty does not disclose, or even suggest, all of the features of claim 1 or claim 4, in particular, with respect to determining the accelerated life test requirements that represent each of the plurality of different types of temperature cycles fluctuations a package/device is expected to undergo over a product lifetime, or incorporating into an accelerated life model quantified expected frequencies and magnitudes of temperature fluctuations of the package/chip device in each of a plurality of temperature regimes over the product lifetime.

It also respectfully submitted that there is no motivation to combine Mencinger and Doty, as suggested by the Office Action, nor is there any motivation to modify the mechanism-based methodology disclosed by Mencinger, in the manner contemplated by claims 1 and 4.

The Office asserts "that a skilled artisan would have made an effort to become aware of what capabilities had been developed in the market place, and hence would have knowingly modified Mencinger with the teachings of Doty" but such assertions are clearly speculative suggestions on the part of the Examiner alone with no supportive basis in the references cited. The cases of In re Fine, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988), and In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992), make plain that if the assertions by the Office reflect a subjective "obvious to try" standard, they do not constitute proper evidence to support an obviousness rejection based on the references relied upon. In particular, the Court in the case of In re Fine stated that:

> Instead, the Examiner relies on hindsight in reaching his obviousness determination. . . . **One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.**

In re Fine, 5 U.S.P.Q.2d at 1600 (citations omitted; emphasis added). Likewise, the Court in the case of In re Jones stated that:

> Before the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. . . .

> **Conspicuously missing from this record is any evidence, other than the PTO's speculation (if it be called evidence) that one of ordinary skill . . . would have been motivated to make the modifications . . . necessary to arrive at the claimed [invention].**

In re Jones, 21 U.S.P.Q.2d at 1943 & 1944 (citations omitted; italics in original). Thus, the proper evidence of obviousness must show why there is a suggestion to combine the references so as to provide the subject matter of the claims and its benefits. Such showing is lacking in the Office Actions to date, and in the Advisory Action.

Moreover, it is respectfully submitted that a *prima facie* case of obviousness has not been made in the present case, since the Office never made any findings, such as, for example, regarding what the ordinary skill level in the art would have been at the time the claimed subject matter of the present application was made. (See In re Rouffet, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998) (the "factual predicates underlying" a *prima facie* "obviousness determination include the scope and content of the prior art, the differences between the prior art and the claimed invention, and the level of ordinary skill in the art")). It is respectfully submitted that the proper test for showing obviousness is what the "combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art," and that the Patent Office must provide particular findings in this regard — the evidence for which does not include "broad conclusory statements standing alone." (See In re Kotzab, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir. 2000) (citing In re Dembiczak, 50 U.S.P.Q.2d 1614, 1618 (Fed. Cir. 1999) (obviousness rejections reversed where no findings were made "concerning the identification of the relevant art," the "level of ordinary skill in the art" or "the nature of the problem to be solved"))). It is again respectfully submitted that there has been no such showing by the Office Actions to date, and in the Advisory Action.

In short, the Office has failed to carry the initial burden of presenting a proper prima facie case of obviousness. (See In re Oetiker, 977 F.2d 1443, 1445, 24, U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992)).

In view of the foregoing, it is respectfully submitted that claims 1 and 4 are allowable.

Claims 2 and 3 depend from claim 1, and are therefore allowable for at least the same reasons as claim 1.

Claim 5 depends from claim 4, and is therefore allowable for at least the same reasons as claim 4.

In view of the foregoing, reversal of the rejection of claims 1 to 5 is respectfully requested.

Claim 16

Claim 16 stands finally rejected under 35 U.S.C. § 103(a) as being obvious over Mencinger in view of Doty. It is respectfully submitted that claim 16 is not rendered obvious over these references for at least the following reasons.

Claim 16 recites features essentially analogous to claim 4, and is therefore allowable for at least the same reasons as claim 4. Moreover, claim 16 further recites quantifying frequencies and magnitudes of temperature fluctuations based in part ***on the shipping route taken by the product***, which is neither disclosed nor suggested by Mencinger and/or Doty. The Office Action asserts that because Appendix A of the Doty reference refers to seasonal variation of the temperature it would be obvious to one skilled in the art at the time the invention was made to model similar temperature relationships based on shipping routes. However, such relationships are clearly not similar, since, for example, the seasonal temperature variations referred to by Doty involve an overall trending of the temperature data occurring over a long period time, rather than an immediate impact as would be expected by the product taking a different shipping route. Hence, the seasonal temperature variation is used by Doty to create a year-long baseline temperature onto which the daily fluctuations are superimposed, rather than quantifying the frequencies and magnitudes of temperature fluctuations pertinent to each identified ambient and power driven temperature fluctuation, as required by claim 16.

In sum, it is therefore respectfully submitted that claim 16 is allowable.

In view of the foregoing, reversal of the rejection of claim 16 is respectfully requested.

B. Claims 6 to 12, 14 and 17 to 22 are not obvious over Mencinger in view of Doty and ReliaSoft.

Claims 6 to 12, 14 and 17 to 22 stand finally rejected under 35 U.S.C. § 103(a) as being obvious over Mencinger in view of Doty, and in further view of Reliasoft. It is respectfully submitted that none of claims 6 to 12, 14 and 17 to 22 is obvious over these references for at least the following reasons.

Claims 6 to 12, 14 and 17 to 22 depend either directly or indirectly from claims 1, 4 and 16, or recite features essentially analogous to at least one of claims 1, 4 and

16, or depend from a claim that recites features essentially analogous to at least of claims 1, 4 and 16, and are therefore allowable for at least the same reasons as claims 1, 4, and/or 16, since the ReliaSoft reference does not cure the critical deficiencies of the Mencinger and Doty references, as explained above.

Further, it is respectfully submitted that the Mencinger and Doty references are not properly combinable with the ReliaSoft reference since there exists no express motivation in any of the references to combine them. In this regard, the Office's assertion that "[t]he motivation would have been that [ReliaSoft] teaches automated reliability calculation based on Inverse Power Law Model ([ReliaSoft]: Page 15, 2nd Figure: Stress Life Relationship) and Coffin Manson empirical formula taught by Mencinger is also inverse power law model" is a mere speculative suggestion on the part of the Examiner, which fails to demonstrate a requisite motivation to modify the Mencinger reference to provide the claimed features, which the Office admits is not disclosed by Mencinger. Indeed, such an assertion does not explain ***why*** a person skilled in the art would be motivated to modify the Mencinger reference. Moreover, the assertion by the Office that the Coffin Manson empirical model is a mere equivalent of any Inverse Power Law model is a drastic over simplification of the technical subject matter described.

In view of the foregoing, reversal of the rejections of claims 6 to 12, 14 and 17 to 22 is respectfully requested.

C. Claim 13 and 15 are not obvious over Mencinger in view of Doty, ReliaSoft and Dellin.

Claims 13 and 15 stands finally rejected under 35 U.S.C. § 103(a) as being obvious over Mencinger in view of Doty, and further in view of ReliaSoft and Dellin. It is respectfully submitted that none of claims 13 and 15 is obvious over these references for at least the following reasons.

Claims 13 and 15 depend indirectly from claim 4, and are therefore allowable for at least the same reasons as claim 4, since the ReliaSoft and Dellin references do not cure the critical deficiencies of the Mencinger and Doty references, as explained above.

Moreover, the assertion by the Office that "[i]t would have been obvious to one (e.g., a designer) of ordinary skill in the art at the time the invention was made to take the Coffin Manson model as described in Dellin and use it with the teachings of Mencinger, Doty and [ReliaSoft] ***to make it more functionally useful***" (emphasis added) is mere hindsight

reasoning and fails to demonstrate a requisite motivation to modify the Mencinger reference to provide the claimed features, which the Office admits is not disclosed by Mencinger.

In view of the foregoing, reversal of the rejections of claims 13 and 15 is respectfully requested.

8. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132. No other evidence has been entered by the Examiner or relied upon by Appellant in the appeal. An "Evidence Appendix" is nevertheless attached hereto.

9. RELATED PROCEEDINGS APPENDIX

As indicated above in Section 2, above, "[t]here are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellant or the assignee, Intel Corporation, 'which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.'" As such, there are no "decisions rendered by a court or the Board in any proceeding identified pursuant to [37 C.F.R. § 41.37(c)(1)(ii)]" to be submitted. A "Related Proceedings Appendix" is nevertheless attached hereto.

10. CONCLUSION

In view of the above, it is respectfully requested that the rejections of claims 1 to 22 be reversed, and that these claims be allowed as presented.

Respectfully submitted,

Dated: 10/27/06

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APPENDIX

1. A computer-implemented method, tangibly embodied on a computer readable storage medium, which when executed will quantify the reliability test requirements of a package/chip device over a product lifetime comprising:

- modeling a plurality of different types of ambient and power-driven temperature cycle fluctuations the package/device is expected to undergo over the product lifetime; and
- determining the accelerated life test requirements that represent each of the plurality of different types of temperature cycles fluctuations.

2. The method of claim 1, wherein the different types of ambient and power-driven temperature cycles are: storage cycles, air shipping cycles, ground shipping cycles, on/idle operation cycles, power on/off, application use cycles within and between program use, and product transfer cycles.

3. The method of claim 1, wherein the test requirements depend upon a market application use of the package/chip device.

4. A method of relating accelerated life test parameters used to assess reliability of a package/chip device to expected frequencies and magnitudes of temperature cycle fluctuations encountered by the package/chip device over a product lifetime, the method comprising:

- defining a particular market application use for the package/chip device;
- quantifying expected frequencies and magnitudes of temperature fluctuations of the package/chip device in each of a plurality of temperature cycle fluctuation regimes, based in part on the particular market application use of the package/chip device; and
- incorporating the quantified expected frequencies and magnitudes of the temperature fluctuations of the package/chip device in each of the temperature regimes into an accelerated life model.

5. The method of claim 4, wherein the ambient and power-driven temperature cycle fluctuation regimes include at least one of:

- storage cycles;
- air shipping cycles;
- ground shipping cycles;
- on/idle cycles;

- within and between application use cycles;
- operator transport cycles;
- power on/off cycles

6. The method of claim 5, further comprising:
   - providing a program interface for receiving user inputs regarding package/chip device design, use, and environmental test chamber parameters;
   - including the user inputs and a warranty life associated with the market application use; and
   - using subroutines to calculate parameters related to use conditions of the package/chip device in the market application by retrieving field data from databases.

7. The method of claim 6, wherein the subroutines include at least:
   - a consumer behavior subroutine that applies information relating to typical consumer behavior associated with the market application specified;
   - an application workload subroutine that applies information relating to power consumption of various typical applications; and
   - an environmental conditions subroutine that applies information relating to both external and internal temperature conditions associated with the market application specified.

8. The method of claim 6, further comprising:
   - estimating ambient temperature fluctuation frequencies for each of the temperature cycle fluctuation regimes over the lifetime of the product based on the user inputs and the parameters calculated by the subroutines; and
   - estimating power driven temperature fluctuation frequencies over the lifetime of the product based on the user inputs and the parameters calculated by the subroutines.

9. The method of claim 8, further comprising:
   - calculating a temperature profile of the package/chip device over the lifetime of the product using the estimated ambient temperature fluctuation frequencies, the estimated power driven fluctuation frequencies, and the parameters calculated by the subroutines;
   - wherein the temperature profile includes a probability density function for each temperature fluctuation regime and the power cycle fluctuations.

10. The method of claim 9, wherein the temperature profiles also include an estimate of rates of temperature change, ramp times and dwell times in each ambient temperature cycle fluctuation regime and in the power driven temperature cycle fluctuations.

11. The method of claim 9, further comprising:

- inputting the user inputs, temperature fluctuation frequencies, and temperature profile into the accelerated life model;
- calculating, according to the accelerated life model, a probability density function of a number of accelerated test cycles required to simulate the temperature fluctuations that occur over the product lifetime; and
- calculating a number of accelerated on/off power cycles required to simulate the on/off power cycle fluctuations that occur over the product lifetime;
- wherein the calculations are based on the input user inputs, temperature fluctuation frequencies, power cycle fluctuation frequencies and temperature profile; and the user inputs which include a power law coefficient and a failure mode type.

12. The method of claim 11, further comprising:

- outputting the temperature profile and the probability density function of the number of accelerated test cycles required to simulate the ambient temperature fluctuations in tabular and graphic form; and
- outputting the probability density function of the number of accelerated on/off power cycles required to simulate the on/off power cycle fluctuations in tabular and graphic form;
- wherein the probability density functions of the number of accelerated test cycles and the number of on/off power cycles required to simulate the temperature fluctuations and on/off power cycle fluctuations indicates respective numbers of accelerated test cycles and accelerated on/off power cycles required to achieve various confidence levels that the package/chip device will not fail over the warranty lifetime.

13. The method of claim 11, wherein the accelerated life model includes a modified Coffin-Manson empirical model.

14. The method of claim 12, wherein the modified Coffin-Manson model calculates a total number of required accelerated test cycles as a sum of usage terms quantifying the stresses contributed by each ambient and power driven temperature cycle fluctuation regime, the

usage terms being equal to the number of temperature fluctuation cycles occurring in each regime multiplied by a temperature fluctuation ratio raised to the power of the power law coefficient.

15. The method of claim 14, wherein the temperature fluctuation ratio includes a material property factor to account for temperature creep and plasticity.

16. A method of systematically quantifying representative field use conditions associated with a particular product having a package/chip device, the method comprising:

- defining a product market segment;
- defining a shipping route taken by the product;
- identifying temperature cycle fluctuations and power cycles fluctuations encountered by the package /chip of the product; and
- quantifying frequencies and magnitudes of temperature fluctuations pertinent to each identified ambient and power driven temperature fluctuation, wherein the frequencies and magnitudes are based in part on the product market segment and the shipping route.

17. The method of claim 16, further comprising:

- extracting information from databases related to customer behavior, application workload, and environmental conditions applicable to the product market segment and shipping route of the product; and
- determining frequencies and magnitudes of ambient and power driven temperature fluctuations for the life of the product based on the extracted information.

18. The method of claim 17, further comprising:

- defining a warranty life of the product; and
- calculating a temperature profile for the package/chip device over the warranty life of the product based on the quantified frequencies and magnitudes of each ambient and power driven temperature fluctuation.

19. An article comprising a computer-readable storage medium which stores computer-executable instructions for causing a computer system to:

- define a particular market application use for the package/chip device;

- quantify expected frequencies and magnitudes of temperature fluctuations of the package/chip device in each of a plurality of temperature cycle fluctuation regimes, based in part on the particular market application use of the package/chip device; and
- incorporate the quantified expected frequencies and magnitudes of the temperature fluctuations of the package/chip device in each of the temperature regimes into an accelerated life model.

20. The article of claim 19, wherein the storage medium stores further instructions for causing a computer system to:

- provide a program interface for receiving user inputs regarding package/chip device design, use, and environmental test chamber parameters;
- include user inputs and a warranty life associated with market application use; and
- process the user inputs in subroutines, the subroutines calculating parameters related to use conditions of the package/chip device in the market application use by retrieving field data from databases.

21. The article of claim 20, wherein temperature fluctuation regimes include at least one of:

(a) storage cycles;
(b) air shipping cycles;
(c) ground shipping cycles;
(d) on/idle cycles;
(e) varied application use cycles;
(f) operator transport cycles; and
(g) power on/off cycles.

22. The article of claim 20, wherein the storage medium stores further instructions for causing a computer system to:

- estimate temperature fluctuation frequencies for each of the temperature cycle fluctuation regimes over the warranty life of the product based on the user inputs and the parameters by the subroutines; and
- calculate a temperature profile of the package/chip device over the warranty life of the product using the estimated temperature fluctuation frequencies and the parameters calculated by the subroutines.

EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132. No other evidence has been entered by the Examiner or relied upon by Appellant in the appeal.

RELATED PROCEEDINGS APPENDIX

As indicated above in Section 2 of this Appeal Brief, "[t]here are no other prior or pending appeals, interferences or judicial proceedings known by the undersigned, or believed by the undersigned to be known to Appellant or the assignee, Intel Corporation, 'which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.' " As such, there are no "decisions rendered by a court or the Board in any proceeding identified pursuant to [37 C.F.R. § 41.37(c)(1)(ii)]" to be submitted.